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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,644	10/20/2003	Ryoko Miyachi	60188-676	1793

7590 05/16/2006

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EXAMINER

KIM, DANIEL Y

ART UNIT	PAPER NUMBER
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2185

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/687,644	Applicant(s) MIYACHI ET AL.	
	Examiner Daniel Kim	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 6-14 and 16-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-14 and 16-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☒ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed March 2, 2006 in response to the PTO Office Action mailed December 2, 2005. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.
2. In response to the last Office Action, claims 1, 2, 6-12 and 16-20 have been amended, claims 5 and 15 has been cancelled, and no other claims have been added. Claims 1-4, 6-14 and 16-20 remain pending in this application.
3. The applicant's amendment filed on March 3, 2006 necessitates new grounds of rejection as presented below in this Office Action.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 6-14 and 16-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2, 6-12 and 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jain et al (US PGPub No. 20030088744).

For claim 1, Jain discloses an information processing method comprising the steps of:

obtaining, among arithmetic instructions, information on data sets referred to by memory reference (data bytes comprise program instructions, whereby the processors fetch instructions from the memory module for execution, par. 0012), and

respectively assigning to different memory banks a plurality of data sets based on the information, each data set being simultaneously referred to in the same memory cycle by memory reference to be performed in accordance with an arithmetic instruction (memory banks operate independently, and processors can simultaneously access different banks of the memory module during the same clock cycle, par. 0013).

For claim 2, Jain discloses establishing bank assignment priority and the assignment to the memory banks is performed in sequence beginning with data sets that are high in priority (a flow control unit determines the priority of access by the processors, if a processor has a higher priority, the unit allows the processor to access the memory while another processor executes a wait state, par. 0020).

Claim 6 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 7, Jain discloses the data sets that are specified to be assigned to the different memory banks are assigned first to the memory banks, then other data are assigned second to the memory banks (data bytes may comprise instructions in a program which are executed in sequence, and a processor would generally access different banks of the memory module after each cycle during program execution, but by synchronizing or staggering the processors to execute the program so that the processors access different memory banks in the same cycle, multiple processors can execute the same program stored in a memory module simultaneously, par. 0016).

Claim 8 is rejected using the same rationale as for the rejections of claims 2 and 6 above.

Claim 9 is rejected using the same rationale as for the rejection of claim 6 above.

Claim 10 is rejected using the same rationale as for the rejection of claim 7 above.

For claim 11, Jain discloses a first unit configured for obtaining information on a plurality of data sets each of which is simultaneously referred to in the same execution cycle by memory reference performed in accordance with an arithmetic instruction (a flow control unit synchronizes the processors to access different memory blocks, par. 0017), and

a second unit configured for assigning the data sets to different memory banks, respectively (the blocks of the memory each have control circuitry to appropriately direct data, par. 0015).

Claim 12 is rejected using the same rationale as for the rejections of claims 2 and 11 above.

Claim 16 is rejected using the same rationale as for the rejection of claim 11 above.

Claim 17 is rejected using the same rationale as for the rejection of claim 11 above.

Claim 18 is rejected using the same rationale as for the rejections of claims 12 and 17 above.

Claim 19 is rejected using the same rationale as for the rejection of claim 16 above.

Claim 20 is rejected using the same rationale as for the rejection of claim 17 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al (US PGPub No. 20030088744) and Chin (US Patent No. 6,247,102).

For claim 3, Jain discloses the invention as per rejection of claim 2 above.

Jain fails to disclose the limitations of the current claim.

Chin, however, helps disclose the bank assignment priority is established according to a loop count that indicates the number of times the arithmetic instruction is executed repeatedly (a read/write data controller with a cache line read/write counter, in which when the last cache line is read from memory, the controller loads the cache line counter with the next count and the next set of memory reads or writes begins, col. 14, lines 23-48 and col. 14, lines 54-67 and col. 15, lines 1-15).

Jain and Chin are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control, especially for the handling of a plurality of memory operations. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a loop count to indicate the number of times an instruction is executed because this allows the next set of memory reads to begin and determine when sufficient read data has been returned from memory so that access to the address/data bus may be moderated accordingly (col. 14, lines 41-44) as taught by Chin.

Claim 13 is rejected using the same rationale as for the rejections of claims 3 and 12 above.

9. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al (US PGPub No. 20030088744) and Idleman (US Patent No. 5,371,855).

For claim 4, Jain discloses the invention as per rejection of claim 2 above.

Jain fails to disclose the limitations of the current claim.

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Idleman, however, helps disclose the bank assignment priority is established according to data-use frequency (a data processing system and cache buffer that may be structured so that a priority system is establish with respect to its frequency of use. The most frequently used information would receive the highest priority and the least frequently used information would receive the lowest priority, col. 2, lines 64-68 and col. 3, lines 1-2).

Jain and Idleman are analogous art in that they are of the same field of endeavor, that is, a system and method for memory management, especially for optimizing bus data transfers. It would have been obvious to a person of ordinary skill in the art at the time of the invention to sort bank assignment priority by data-use frequency, because this would allow for rapid access of priority information and enhance system performance (col. 2, lines 56-58), as taught by Idleman.

Claim 14 is rejected using the same rationale as for the rejections of claims 4 and 12 above.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

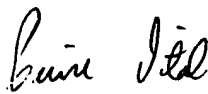
Contact Information

11. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

5-8-06


PIERRE VITAL
PRIMARY EXAMINER